Trade-off Study of Heat Sink and Output Filter Volume in a GaN HEMT Based Single Phase Inverter

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***Abstract*—This paper presents the trade-off study of heat sink and output filter volume of a GaN HEMT based single phase inverter. The selected topology is three-level Active Neutral point Clamped (ANPC) inverter, and the main aim is to explore the benefits of the GaN HEMTs at 600 V blocking class on the system level efficiency, and power density under wide range of operating conditions. The paper starts by introducing the inverter topology, selected PWM scheme and followed by the device features, static and dynamic characterisation and continues with presenting and discussing the results of extensive experimental and analytical characterisation. After this, the impact of GaN HEMTs on inverter volume is discussed in terms of heat sink and output filter volume analysis under different switching frequency and heat sink temperature conditions. The calculation of heat sink volume and single stage LC output filter volume are presented with respect to experimental results of single phase prototype. The findings from static, dynamic characterisation and single phase prototype results clearly show that GaN HEMT has excellent switching performance under wide load current and heat sink temperature conditions. The high performance of the inverter lead to reduction of the combined total volume, including output filter and heat sink volume.**

***Index Terms*—Keywords–Wide bandgap (WBG) power devices, gallium-nitride (GaN), HEMT, three-level active neutral point clamped (3L-ANPC) converter, photovoltaic (PV) systems**

I. Introduction

WIDE-BANDGAP (WBG) devices gained immediate attention in power electronic community due to superior switching and conduction properties in comparison to Silicon (Si). The literature review clearly shows that SiC and GaN devices are promising advancements in power semiconductor technology that can enable high efficiency and high power density by increased switching frequencies [1], [2].

Normally-off p-gate GaN HEMTs have been introduced by Panasonic at 600V blocking class. The devices have been used in different applications such as resonant LLC DC/DC converter, three phase inverter, synchronous buck converter and three level inverters that show the high switching and conduction performance of the devices in different operating conditions [3]–[6]. The GaN HEMTs at 600 V blocking class gained more attention from researches with the announcement of Little Box Challenge [7] in 2015, where the aim of the challenge is to design a 2 kVA, single phase inverter with more than 3 kW per litre power density and 95 $\%$ efficiency based on weighted CEC weighted efficiency. Various full-bridge topologies have been compared including soft-switching and hard switching topologies based on enhancement mode GaN HEMT and SiC MOSFET [8], [9]. The switching frequency of the converters range between 100 kHz to 200 kHz to reduce output filter size while keeping the inverter efficiency above 95 $\%$. A multilevel inverter topology based on 200 V GaN devices and achieving MHz effective switching frequency at the output of the inverter is presented in [10]. In addition to inverter applications, active power decoupling converters to eliminate electrolytic capacitors in single phase inverters have been also discussed and realised with these WBG devices. The comparison of various topologies based on high frequency switching WBG devices is presented in [11] and [12].

In this paper, the analysis, trade-off study of heat sink and output filter volume in a GaN HEMT based single phase Active Neutral point Clamped (ANPC) inverter is presented. The structure of the paper is as follows: In Section II, the ANPC topology and principle of operation is presented. In Section III, the characterisation of GaN HEMT including static and dynamic performance under different operating conditions are presented. In Section IV, the details of the prototype and test conditions are presented. In Section V, experimental results of the single phase prototype under various operating conditions are presented including inverter efficiency and loss breakdown under different operating conditions. Finally, in Section VI, the impact of GaN HEMT on converter volume including output filter and heat sink volume is presented and discussed.

II. ANPC Topology and PWM Scheme

Two level inverters such as standard half-bridge inverter, or full-bridge inverter with bipolar modulation can provide two level output waveform with high performance, but also with the penalty of high dV/dt stress and large output filter volume. The high dV/dt across the output and semiconductor devices, and large output filter volume lead the engineers to propose multi level topologies with higher number of switches and innovative switching schemes. Among the proposed solutions, three level inverters such as ANPC have gained attention due to simplicity, lower component count in comparison to five or seven level topologies and high efficiency [13], [14]. Due

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TABLE I: Switching States

Output State	S_1	S_2	S_3	S_4	S_5	S_6
$+V_{DC}$	1	0	1	1	0	0
0_P	0	1	1	0	0	0
0_N	0	0	0	1	1	0
0_{PN}	0	1	1	1	1	0
$-V_{DC}$	0	1	0	0	1	1

to its high efficiency, low component count and suitability for GaN HEMT devices, which will be explained in the following sections, ANPC is chosen as the topology to study the trade off between power cell efficiency, heat sink volume and output filter volume in a GaN HEMT based single phase inverter system.

The ANPC inverter is a member of half-bridge neutral point clamped inverter family, and it was introduced in [15], [16] as an alternative to neutral point clamped (NPC) inverter for improved loss balancing and better utilization of semiconductor chip areas in the inverter and is of widespread use, for instance, in renewable energy (e.g., wind, PV) and industrial drive applications [15]–[18]. The ANPC topology is selected for this study as it is shown in literature that NPC based topologies provide high efficiency with three level output voltage waveform with devices at 600 V blocking class for 230 V grid systems [19], [14]. The schematic of the converter is shown Fig. 1a.

Different modulation strategies have been discussed for the ANPC inverter in order to achieve a balanced switching loss distribution or doubling of the effective switching frequency at the output [20]. Solutions proposed in [17], [18], [21], [22] are limited to the use of Si devices and were optimised for IGBTs as well as for MOSFETs. GaN HEMT devices do not require anti parallel diode due to intrinsic reverse conduction capability and suitable for parallel conduction at any switching state unlike IGBTs. A modulation strategy based on reverse conduction capability of SiC MOSFETs and GaN HEMTs has been introduced in [19], [23], and presented in Fig. 1b. The positive voltage is applied to the output of by turning-on S_1 and S_3 and the output current flows through the two devices in series. During the positive active-state, S_4 ensures an equal DC-link voltage sharing between S_5 and S_6 without conducting any current. The transition from positive active-state to zero-state is accomplished by switching S_1 off, and then simultaneously switching S_2 and S_5 on, and thus the current is divided in two parallel paths: S_2-S_3 and S_4-S_5. Same commutation scheme is used for complementary switches during the negative active-state and the zero-state. This modulation method ensures low conduction losses at zero-states, and the outer switches (S_1 and S_6) are exposed to switching losses at unity power factor. The resulting output states are summarised in Table I; the synchronous rectification capability of the transistors is utilised during zero state conduction.

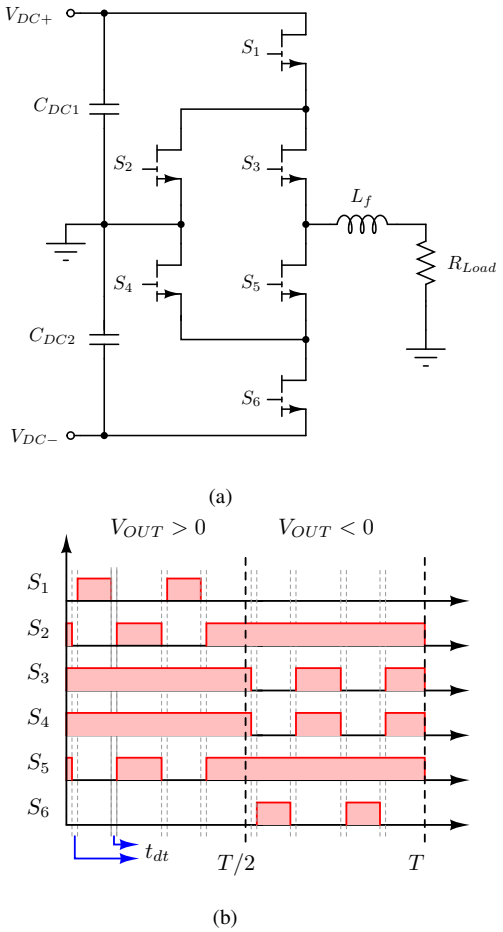


Fig. 1: a) Schematic of 3-level ANPC inverter with inductive load and b) Optimised PWM signals for ANPC inverter with dead time.

III. GaN HEMT Characterisation

The devices used in this work are Panasonic PGA26C09DV, in TO-220 package. The device parameters are presented in Table II. The device is rated at 15 A continuous current at 25 °C case temperature with 71 mΩ on-state resistance $R_{DS_{ON}}$. It has small input capacitance C_{iss} and reverse transfer capacitance C_{oss} which provides fast switching performance. In addition to this, small gate charge leads to low gate driver

TABLE II: PGA26C09DV GaN HEMT Parameters

Drain-Source Voltage (V_{DS})	600 V
Continuous Drain Current (I_{DS})	11 A @ 100 °C
Drain-Source On-State Resistance ($R_{DS_{ON}}$)	71 mΩ @ 25 °C
Input Capacitance (C_{iss})	272 pF
Output Capacitance (C_{oss})	199 pF
Reverse Transfer (C_{rss})	32 pF
Gate Charge (Q_g)	6.5 nC
Min. Gate Threshold Voltage (V_{th})	1.2 V
Gate-Source Voltage (V_{GS})	-10 to +4.5 V
Maximum Junction Temperature (T_j)	150 °C
Device Package	TO-220D

loss [6]. Apart from the datasheet values, the static and dynamic characterisation of the device is conducted under different device current and heat sink temperature values with a controlled current source and a temperature controlled heat sink. The measured on-state characteristics, in both forward and reverse conduction with different gate-source voltage V_{GS}, are shown in Fig. 3.

Although there is no physical body diode in GaN HEMTs, reverse conduction, from source to drain, is enabled by the symmetrical device design. Reverse conduction starts when the gate-drain voltage, V_{GD}, exceeds the gate-drain threshold voltage $V_{GD,TH}$; the required voltage to activate reverse conduction is then [24]:

$$V_{GD} = V_{GS} - V_{DS} > V_{GD,TH} \tag{1}$$

In principle, $V_{GD,TH}$ equals the gate-source threshold voltage, $V_{GS,TH}$, which is typically the parameter specified in the datasheet [24]. Therefore, for the on-state voltage drop during reverse conduction, the equality holds:

$$V_{SD} = I_D \cdot R_{SD,REV} - (V_{GS} - V_{GS,TH}) \tag{2}$$

where I_D is the drain current and $R_{SD,REV}$ is the effective on-state resistance during reverse conduction. The transistors have relatively low threshold voltage and so, application of negative V_{GS} bias is recommended for turn-off. As evident from Fig. 3 and Eq. 2, a negative V_{GS} value increases V_{SD}, increasing the losses associated with the freewheeling action. Use of external anti-parallel diodes (e.g., SiC Schottky devices) may help improving reverse conduction performance, but negatively affects the switching performance, in reason of increased equivalent output capacitance of the device. Thus, in this work it was decided to just use the transistors and to apply synchronous rectification, that is, to limit reverse conduction with negative gate-source bias only to the dead-times in between commutations, which were minimised for maximum performance. Moreover, the turn-off gate bias voltage was not kept constant at a negative value, but rather decreased in amplitude during the off-time to maximise the switching performance, as shown in Fig. 2b and with the gate drive circuitry presented in Fig. 2a and discussed in [6].

Well known double pulse test circuitry is used to evaluate the hard switching performance of the GaN HEMT under different temperature and device current conditions. The blocking voltage is set to 350 V (half of total DC link voltage in a half bridge based inverter). The representative switching waveforms are reported in Fig. 4. Two conditions are analysed: normal operation (labelled "GaN HEMT", shown in Fig. 2b), where the device is turned-off with $V_{GS} = -6$ V and turned-on again when $V_{GS} = -4$ V; and zero-voltage turn-on operation (labelled as "GaN HEMT-z", shown in Fig. 2b) where the device is turned-off still with -6 V, but it is then turned on again starting from $V_{GS} = 0$ V. In other words, during turn-on, in "GaN HEMT" case, the gate-source voltage is changed from -4 V to 3.2 V, and in "GaN HEMT-z" case, the gate-source voltage is changed from 0 V to 3.2 V. It can be seen that the fall time of drain source voltage V_{DS} is around 26 ns with "GaN HEMT-z" condition, and approximately two

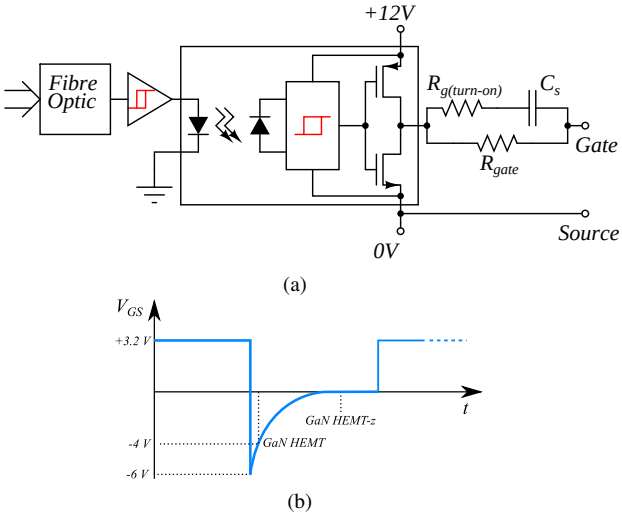


Fig. 2: a) Schematic of GaN HEMT driver and b) illustration of applied gate-source drive voltage waveform.

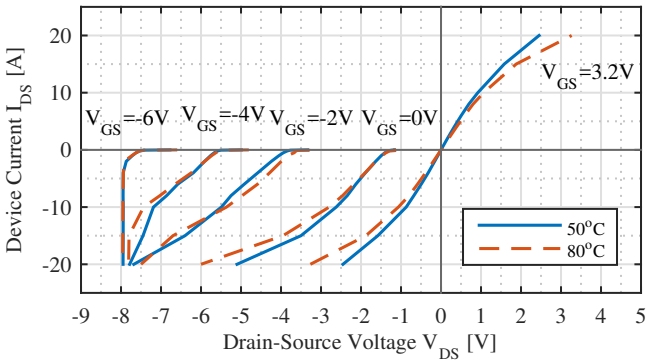


Fig. 3: Measured output characteristics of the GaN transistors measured at different temperatures.

times faster than the one with "GaN HEMT". At turn-off transient, the rise time of V_{DS} is approximately 20 ns for both cases. As evident from Fig. 3, applying a negative turn-off bias voltage longer than strictly necessary slows down the turn-on transition and decreases the switching performance. So, the gate-driver design and free-wheeling operation are important design optimisation aspects and different decay rates in the negative portion of V_{GS} can be used in combination with different switching frequencies.

Finally, the turn-on switching energies E_{on}, E_{on-z}, and turn-off switching energies E_{off}, E_{off-z} for GaN HEMT are calculated at different device current I_{DS} and heat sink temperature conditions. The turn-on and turn-off switching energies under different device current conditions at 60 °C heat sink temperature are presented in Fig. 5a, and under different heat sink temperatures at 16 A device current are presented in Fig. 5b. It can be seen from Fig. 5a that the switching energies increase linearly with I_{DS} and the turn-on energy E_{on} can increase up to three times with negative voltage at high I_{DS} conditions. On the other hand, regarding temperature dependency in Fig. 5b, the turn-on energy increases by a factor of 1.06 for both conditions and the turn-off energy decreases by a factor of 1.03 with the temperature increase from 50 °C

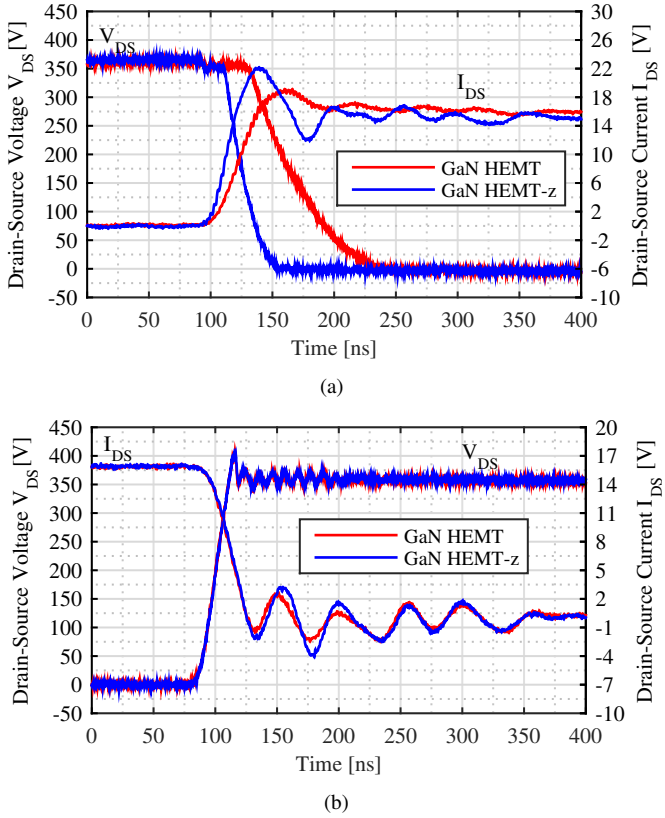


Fig. 4: Measured switching current and voltage waveforms during the turn-on (a) and turn-off (b) transitions.

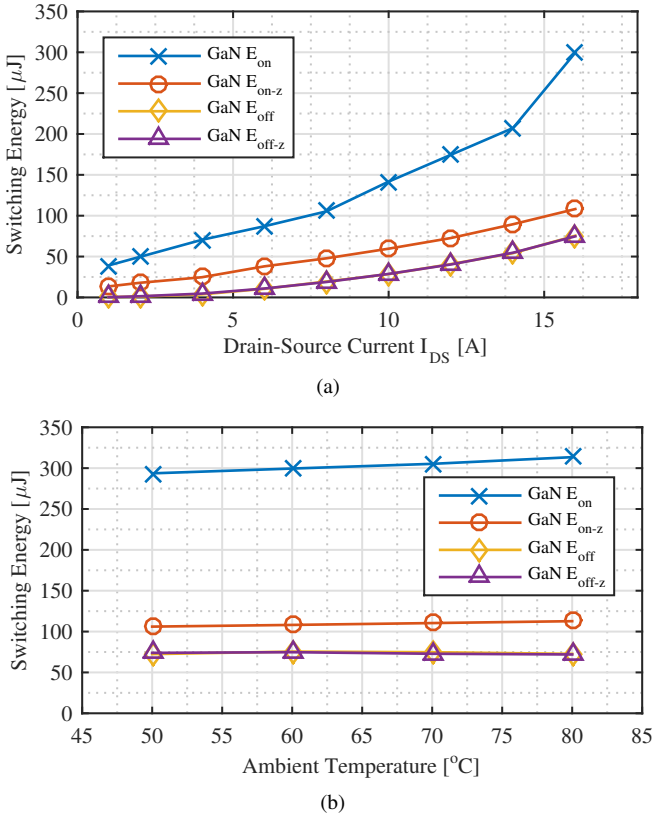


Fig. 5: Measured switching energies versus drain-source current at 60 °C (a) and heat sink temperature (b) at 16 A drain-source current.

to 80 °C.

IV. ANPC Inverter Prototype

The single phase inverter prototype is shown in Fig. 6a, along with the main design and test parameters presented in Table III. It embeds the fiber optic receivers for transfer of PWM signals from an FPGA board, individual isolated gate drivers for each switch, film decoupling capacitors and a temperature controlled thermal management device, consisting of two cooling fans and two heating resistors mounted at the sides of a heat-sink to decouple the parametric temperature study from load conditions and switching frequency. With respect to any selected switching strategy, S_1 or S_3 may be subject to switching losses for positive output voltage and positive output current. In the selected switching strategy presented in Fig. 1b, S_1 and S_6 switches will be subject to switching losses at positive and negative halves of the output waveform respectively with unity power factor operation. The total commutation inductance formed by the commutation loop stray inductance L_σ and the DC-link capacitor self-inductance L_{DC1}, as shown in Figs. 7a and 7b for different commutation loops, as to be minimised for reducing voltage overshoots and switching losses [25]. The self-inductance of DC-link capacitor can be minimised by paralleling high frequency capacitors (e.g., ceramic, film) and commutation loop inductance can be minimised by placing conductors that carry opposing currents in adjacent layers to induce magnetic field self-cancellation. Based on these principles, the prototype

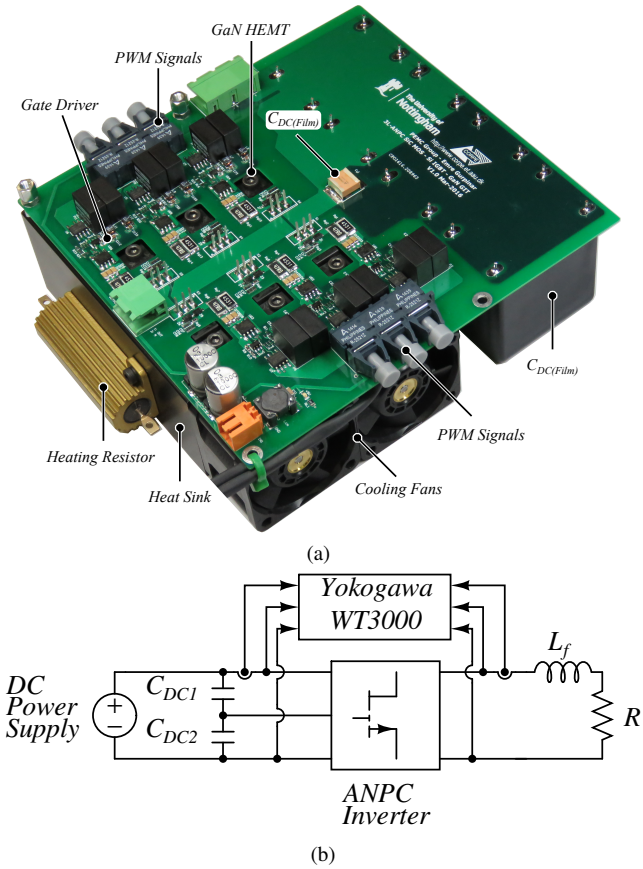


Fig. 6: a) Single phase GaN HEMT based ANPC inverter and b) test setup for GaN HEMT based ANPC inverter.

PCB has been designed in order to minimise the commutation loop between commutating switches S_1-S_5, S_1-S_2, and S_6-S_3, S_6-S_4. The PCB consists of four layers with 0.2 mm FR4 insulation between layers and 1 μF, 400 V CeraLink capacitors from TDK as decoupling capacitors C_{DC1} and C_{DC2}, shown in Fig. 7 [26].

A simple RL load is used here for evaluation of performance under different operational conditions. The efficiency of the power cell is measured with a Yokogawa WT3000E precision power analyser, which provides adequate accuracy within the switching frequency range in this work [27]. The inverter was tested under a very broad variety of operational conditions, changing the output power delivery between 300 W and 2 kW, the switching frequency between 16 kHz and 160 kHz and the heat-sink temperature between 50 °C and 80 °C.

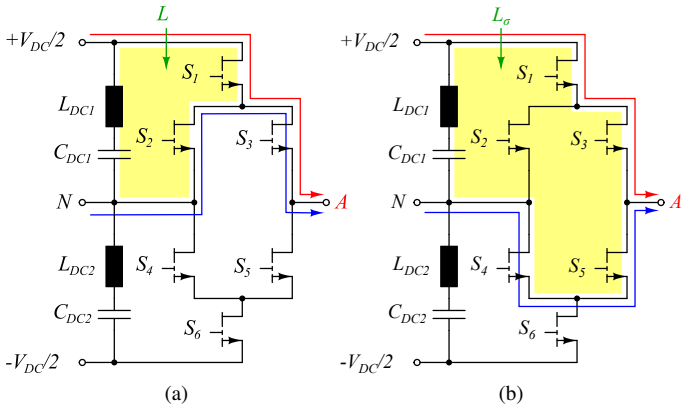


Fig. 7: Commutation loops in the 3L-ANPC from positive to neutral states: a) positive state to upper neutral state and b) positive state to lower neutral state [25].

TABLE III: Prototype Parameters

Maximum Output Power (P_{MAX})	2 kW
DC Link Voltage (V_{DC})	700 V
Output RMS Voltage (V_{OUT})	230 V
Output Filter Inductance (L_f)	1.6 mH
DC Link Capacitance (C_{DC})	4 mF
Switching Frequency (f_s)	16 kHz to 160 kHz
Dead-time (t_{dt})	186 ns
Heat Sink Temperature (T_h)	50 °C to 80 °C

V. Experimental Results and Loss Analysis

The inverter is tested at 120 different operating points to evaluate the performance with 4 heat sink temperatures (50 °C, 60 °C, 70 °C and 80 °C), 5 switching frequencies (16 kHz, 32 kHz, 64 kHz, 128 kHz and 160 kHz) and 6 output load conditions (300 W , 450 W, 850 W, 1250 W, 1650 W and 2 kW). The efficiency and power loss of the inverter at 50 °C heat sink temperature under various load and switching frequency conditions are presented in Figs. 8a and 8b respectively. The superior switching performance of GaN HEMTs provide very high efficiencies (above 99 %) at low switching frequencies. The efficiency of the power cell reduces gradually due to increase in switching loss as the switching frequency is increased and the efficiency stays above 97 % under wide load region at 128 kHz. In terms of power loss, as the switching frequency of the inverter is increased by a factor of 4 (16 kHz to 64 kHz), the power loss increases only by a factor of 1.5. If the switching frequency is increased to 128 kHz (increase by factor of 8), the losses increase by a factor of 2.

The efficiency and power loss curves with respect to switching frequency at 2 kW output power are presented in Figs. 9a and 9b respectively. The efficiency decreases linearly with increase of switching frequency from 98.5 % to 96.5 % at 50 °C case temperature. The temperature dependency of the efficiency is presented in Fig. 10 at 2 kW output power and

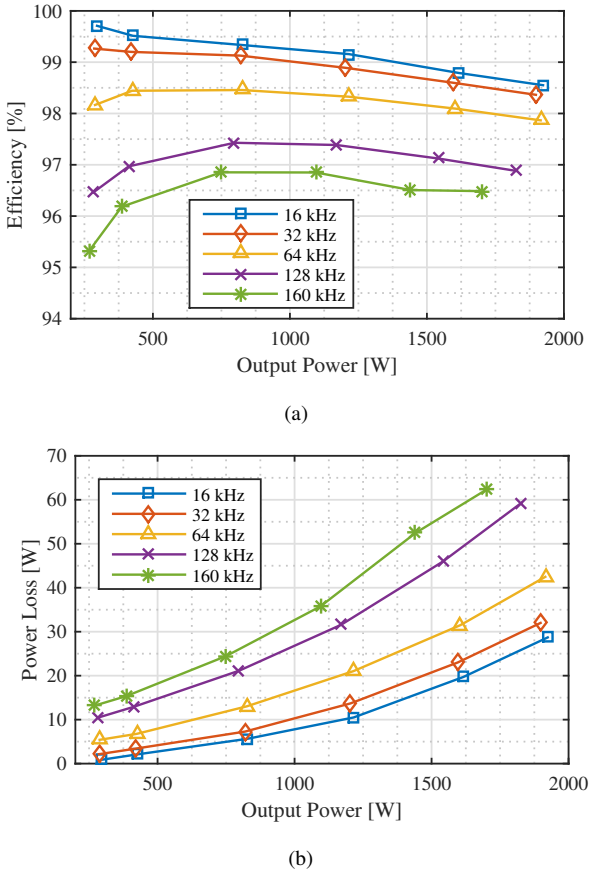


Fig. 8: Performance of GaN HEMT based ANPC power cell versus output power at 50 °C heat sink temperature: a) efficiency, b) power loss.

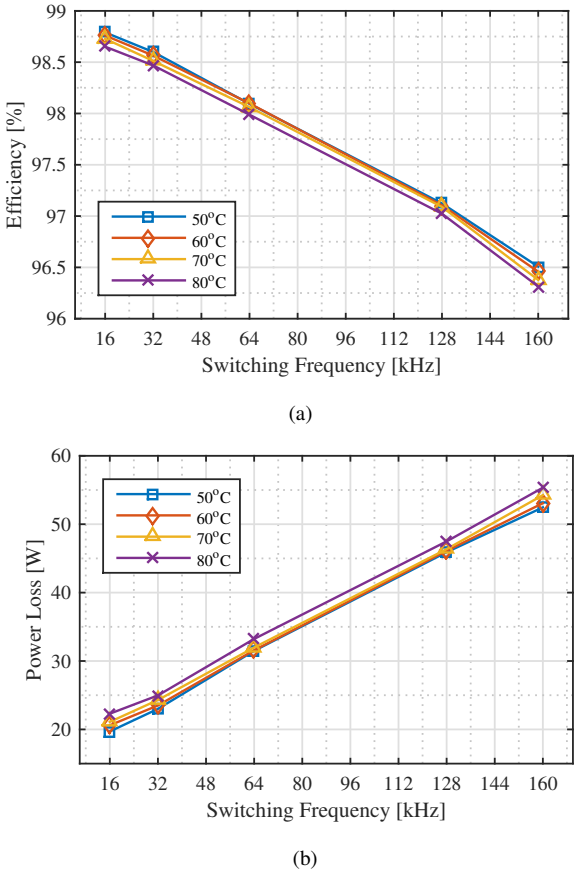


Fig. 9: Performance of GaN HEMT based ANPC power cell versus switching frequency at 2 kW output power: a) efficiency, b) power loss.

5 different switching frequencies. The results in Figs. 9a and 9b show that the performance of the power cell has minimum dependency to heat sink temperature within the test conditions and high efficiency can be maintained with increased switching frequency. The increase of switching frequency and heat sink temperature will allow the designer to reduce the output filter and heat sink volume, which will be discussed in the following sections.

A. Loss Breakdown

The breakdown of total power cell loss in terms of conduction and switching losses is conducted to evaluate the dominant loss component at different switching frequency and heat sink temperature conditions. In order to separate conduction and switching losses for each operating point, conduction losses with respect to output load, dead-time and heat sink temperature are calculated based on the on-state performance of GaN HEMT, which was discussed in Section III. Then, the calculated conduction loss value is subtracted from experimental power cell loss value for each operating point, which was presented in the previous section, to obtain the total switching loss.

The conduction losses are calculated based on sinusoidal approximated output voltage and current, excluding switching ripple current and harmonics. The approximated output voltage and current waveforms for this analysis are illustrated in Fig. 11. The PWM switching waveforms for the selected modulation scheme including dead-time t_{dt} between complimentary devices are presented in Fig. 1b. An arbitrary phase shift ϕ between output voltage and current is shown to derive conduction loss equations for any power factor condition. The output current in Fig. 11 can be expressed as:

$$i(t) = \widehat{I}_{OUT} \cdot sin(\omega t - \phi) \tag{3}$$

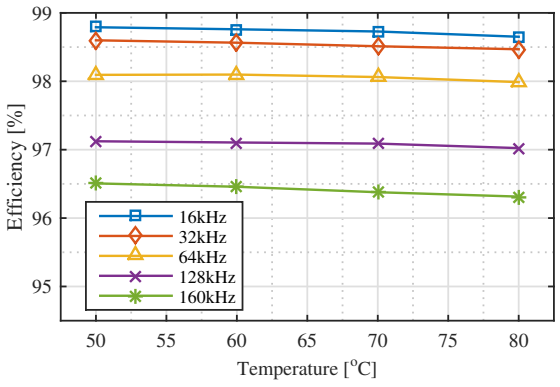
where $\widehat{I}_{OUT}$ is the output current amplitude. The conduction time of each device can be expressed by duty cycle D. The duty cycle for active states ($+V_{DC}/2$ or $-V_{DC}/2$), D_{active} can be expressed as [19]:

$$D_{active}(t) = M \cdot sin(\omega t) \tag{4}$$

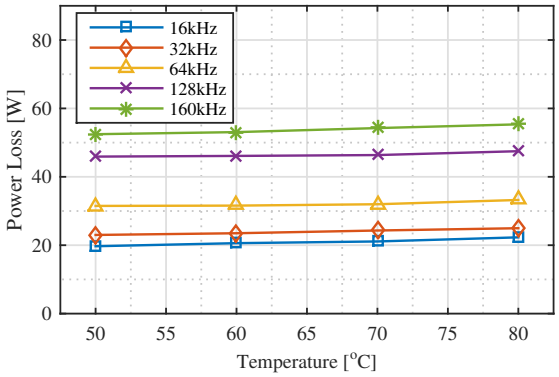
where M is the modulation index varying between 0 and 1. Therefore the duty cycle for zero states D_{zero} can be calculated as follow:

$$D_{zero}(t) = 1 - M \cdot sin(\omega t) \tag{5}$$

The on-state voltage drop across and therefore conduction loss



(a)



(b)

Fig. 10: Performance of GaN HEMT based ANPC power cell versus heat sink temperature at 2 kW output power: a) efficiency, b) power loss.

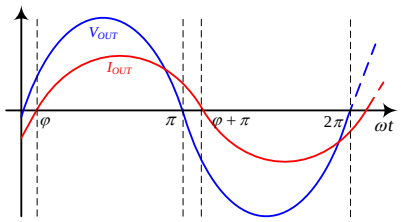


Fig. 11: a) Approximated output voltage and current waveforms for loss analysis and b) PWM signals for ANPC inverter with dead-time.

at active state can be calculated as follow:

$$v_{on}(t) = R_{DS} \cdot i(t) \tag{6}$$

$$P_{cond_a} = \frac{1}{2\pi}\int_0^{\pi} i(t) \cdot v_{on}(t) \cdot D_{active}(t) \cdot \mathrm{d}(\omega t) \tag{7}$$

$$P_{cond_a} = \frac{\widehat{I}_{OUT}^2 \cdot R_{DS} \cdot M}{2\pi} \cdot \left(1 + \frac{cos(2\phi)}{3}\right) \tag{8}$$

where R_{DS} is on-state resistance at given temperature. Similarly the conduction loss at zero state can be calculated:

$$P_{cond_z} = \frac{1}{2\pi}\int_0^{\pi} i(t) \cdot v_{on}(t) \cdot D_{zero}(t) \cdot \mathrm{d}(\omega t) \tag{9}$$

$$P_{cond_z} = \frac{\widehat{I}_{OUT}^2 \cdot R_{DS}}{2\pi} \cdot \left(\frac{\pi}{2} - M \cdot \left(1 + \frac{cos(2\phi)}{3}\right)\right) \tag{10}$$

As it is shown in Fig. 1b, there is dead-time between complementary switches S_1-$S_{2,5}$ and S_6-$S_{3,4}$ to avoid shoot through. After the conducting device is turned off, the complementary device will start conducting the output current in reverse conduction mode with higher on-state losses during dead-time. As shown in Section III, GaN HEMT devices have diode like conduction characteristic in reverse conduction mode when gate-source voltage is below threshold of the device. Therefore, the on-state voltage drop across GaN HEMT, v_{dt}, during dead-time can be expressed with the following equation:

$$v_{dt}(t) = -V_f + \widehat{I}_{OUT} \cdot R_{DS} \cdot sin(\omega t - \phi) \tag{11}$$

where V_f is on-state threshold voltage and can be neglected when the device is turned-on. Based on Eq. 11, the dead-time conduction loss for 0 to ϕ region in Fig. 11 is:

$$P_{dt_{1-bp}} = \frac{1}{2\pi}\int_0^{\phi} v_{dt}(t) \cdot i(t) \cdot t_{dt} \cdot 2 \cdot f_{sw} \cdot \mathrm{d}(\omega t) \tag{12}$$

$$\begin{aligned} P_{dt_{1-bp}} = \frac{t_{dt} \cdot f_{sw}}{\pi} \Big[& V_f \cdot \widehat{I}_{OUT} - V_f \cdot \widehat{I}_{OUT} \cdot cos(-\phi) \\ & + \widehat{I}_{OUT}^2 \cdot R_{DS} \left(\frac{\phi}{2} - \frac{1}{4} sin(2\phi)\right)\Big] \end{aligned} \tag{13}$$

$$P_{dt_{1-up}} = \frac{1}{2\pi}\int_0^{\phi} v_{dt}(t) \cdot i(t) \cdot t_{dt} \cdot 2 \cdot f_{sw} \cdot \mathrm{d}(\omega t) \tag{14}$$

$$P_{dt_{1-up}} = \frac{t_{dt} \cdot f_{sw}}{\pi} \left[\widehat{I}_{OUT}^2 \cdot R_{DS} \left(\frac{\phi}{2} - \frac{1}{4} sin(2\phi)\right)\right] \tag{15}$$

where $P_{dt_{1-bp}}$ corresponds to dead-time conduction loss when the gate-source voltage is below threshold and $P_{dt_{1-up}}$ corresponds to dead-time conduction loss when the device is turned-on. Similarly, the dead-time conduction loss for ϕ to π region in Fig. 11 is:

$$P_{dt_{2-bp}} = \frac{1}{2\pi}\int_{\phi}^{\pi} v_{dt}(t) \cdot i(t) \cdot t_{dt} \cdot 2 \cdot f_{sw} \cdot \mathrm{d}(\omega t) \tag{16}$$

$$\begin{aligned} P_{dt_{2-bp}} = \frac{t_{dt} \cdot f_{sw}}{\pi} \Bigg[& \frac{V_f \cdot \widehat{I}_{OUT}}{2} \left(cos(\pi - \phi) - 1\right) \\ & + \frac{\widehat{I}_{OUT}^2 \cdot R_{DS}}{4} \left(\frac{\pi - \phi}{2} + \frac{1}{4} sin(2\phi)\right)\Bigg] \end{aligned} \tag{17}$$

$$P_{dt_{2-up}} = \frac{1}{2\pi}\int_{\phi}^{\pi} 2 \cdot v_{dt}(t) \cdot i(t) \cdot t_{dt} \cdot 2 \cdot f_{sw} \cdot \mathrm{d}(\omega t) \tag{18}$$

$$P_{dt_{2-up}} = \frac{t_{dt} \cdot f_{sw}}{\pi} \left[\frac{\widehat{I}_{OUT}^2 \cdot R_{DS}}{4} \left(\frac{\pi - \phi}{2} + \frac{1}{4} sin(2\phi)\right)\right] \tag{19}$$

Dead time t_{dt} also means reduction of conduction time as the applied total gate pulse time is reduced by dead-time duration. The reduction of power loss in a switch can be calculated as follow:

$$P_{dt_{red}} = \frac{1}{2\pi}\int_0^{\pi} R_{DS} \cdot \widehat{I}_{OUT}^2 \cdot sin^2(\omega t - \phi) \cdot t_{dt} \cdot f_{sw} \cdot \mathrm{d}(\omega t) \tag{20}$$

$$P_{dt_{red}} = \frac{t_{dt} \cdot f_{sw} \cdot R_{DS} \cdot \widehat{I}_{OUT}^2}{4} \tag{21}$$

The absence of V_f can be seen in Eqs. 20 and 21 as the reduction occurs when the device is turned-on. The conduction cases for switches S_1, S_2 and S_3 for unity and zero power factor cases are presented in Fig. 12 based on Fig. 1b. The *Control Signal* represents the PWM signal before applying dead-time to the gate signal, $P_{dt_{red}}$ is the reduction in conduction loss expressed in Eq. 21, $P_{cond_{S_x}}$ is the total conduction loss across specified switch, $P_{cond_{ON}}$ is the conduction loss when the specified device is turned-on and $P_{dt_{x-bp}}$ is the dead-time loss when gate voltage is below threshold as presented in Eqs. 13 and 17.

It can be seen from Figs. 12a and 12d that S_1 only conducts during the positive voltage output in ANPC inverter. The actual control signal is reduced by introduction of dead-time and the total loss $P_{cond_{S1}}$ is equal to $P_{cond_{ON}}$ at unity power factor as the output voltage V_{OUT} is clamped to zero state during dead-time and no current flows through S_1. At 0 power factor, during dead-time, the output current I_{OUT} flows through S_1 and V_{OUT} is clamped to $V_{DC}/2$. Therefore the $P_{cond_{S1}}$ is equal to sum of $P_{cond_{ON}}$ and $P_{dt_{1-bp}}$. For arbitrary power factor, the total conduction loss across S_1 $P_{cond_{S1}}$ can be expressed by using Eqs. 8, 13 and 21, as:

$$P_{cond_{S_1}} = P_{cond_a} + P_{dt_{1-bp}} - P_{dt_{red}} \tag{22}$$

With similar approach, the conduction loss of S_2 for arbitrary power factor can be calculated. As the S_2 conducts at both positive half and negative half of output voltage, the total conduction loss of S_2 can be calculated as the sum of positive half conduction loss P_{S_2+} and negative half conduction loss P_{S_2-}:

$$P_{cond_{S_2}} = P_{S_2+} + P_{S_2-} \tag{23}$$

where P_{S_2+} and P_{S_2-} are defined as follow:

$$P_{S_2+} = \frac{P_{cond_z}}{4} + P_{dt_{2-bp}} - \frac{P_{dt_{red}}}{4} \tag{24}$$

$$P_{S_2-} = \frac{P_{cond_z}}{4} + P_{dt_{2-up}} - \frac{P_{dt_{red}}}{4} \tag{25}$$

The only difference between P_{S_2+} and P_{S_2-} is the dead-time conduction losses $P_{dt_{2-bp}}$ and $P_{dt_{2-bp}}$. As it can be seen from Figs. 12b and 12e, $P_{dt_{2-bp}}$ corresponds to reverse conduction dead-time losses at the positive half of the output when the device is turned-off, and $P_{dt_{2-up}}$ corresponds to increased conduction time in $P_{cond_{ON}}$ at the negative half of the output voltage. It should be noted that P_{cond_z} and $P_{dt_{red}}$ are divided by 4 as the output current is divided into two parallel conduction paths: S_2-S_3 and S_4-S_5. Similarly, according to Figs. 12c and 12f, the conduction loss of S_3 for arbitrary power factor can be calculated as:

$$P_{cond_{S_3}} = P_{S_3+} + P_{S_3-} \tag{26}$$

where P_{S_3+} and P_{S_3-} are conduction losses at positive half and negative half of output voltage respectively. At positive half of the output voltage, S_3 is completely on and therefore will at both active and zero states. Based on $P_{cond_{S_1}}$ in Eq. 22 and P_{S_2+} in Eq. 24 and considering that S_3 is turned-on at dead-time instants, the conduction loss of S_3, P_{S_3+}, can be expressed as:

$$P_{S_3+} = P_{cond_a} + \tfrac{P_{cond_z}}{4} + P_{dt_{1-up}} + P_{dt_{1-up}} - \tfrac{5 \cdot P_{dt_{red}}}{4} \tag{27}$$

At the negative half of output voltage, as shown in Figs. 12b, 12e, 12c and 12f, the loss profile of S_3 is same as the loss profile of S_2 at the positive half of output voltage. Therefore, based on Eq. 24, P_{S_3-} is:

$$P_{S_3-} = \frac{P_{cond_z}}{4} + P_{dt_{2-bp}} - \frac{P_{dt_{red}}}{4} \tag{28}$$

With symmetrical output current and voltage waveforms (e.g. no DC offset, no overmodulation), the total conduction loss P_{cond_t} in one fundamental cycle can be calculated as:

$$P_{cond_t} = 2 \cdot \left(P_{cond_{S_1}} + P_{cond_{S_2}} + P_{cond_{S_3}}\right) \tag{29}$$

The loss figures for five different switching frequencies and four different heat sink temperatures at 1.3 kW output power in terms of total, switching and conduction losses are presented in Figs. 13a, 13b and 13c respectively. As it is shown in previous section, the total loss increases with respect to increase in switching frequency, and it can be seen in Fig. 13c that main contributor to this is the increase in switching loss. At low switching frequencies such as 16 kHz and 32 kHz, the total power cell loss is dominated by conduction loss. At 64 kHz, the switching loss is at the same range with conduction loss and dominates the total power cell loss at 128 kHz and 160 kHz switching frequencies. The switching loss is independent from heat sink temperature and the conduction loss increases gradually with the increase of R_{DS}. One thing to note in Fig. 13b is the increase of conduction loss with the increase of switching frequency. This is due to the increase of proportion of dead-time in a switching period which increases the dead-time losses linearly in Eqs. 13, 15, 17 and 19 with $t_{dt} \cdot f_{sw}$ term.

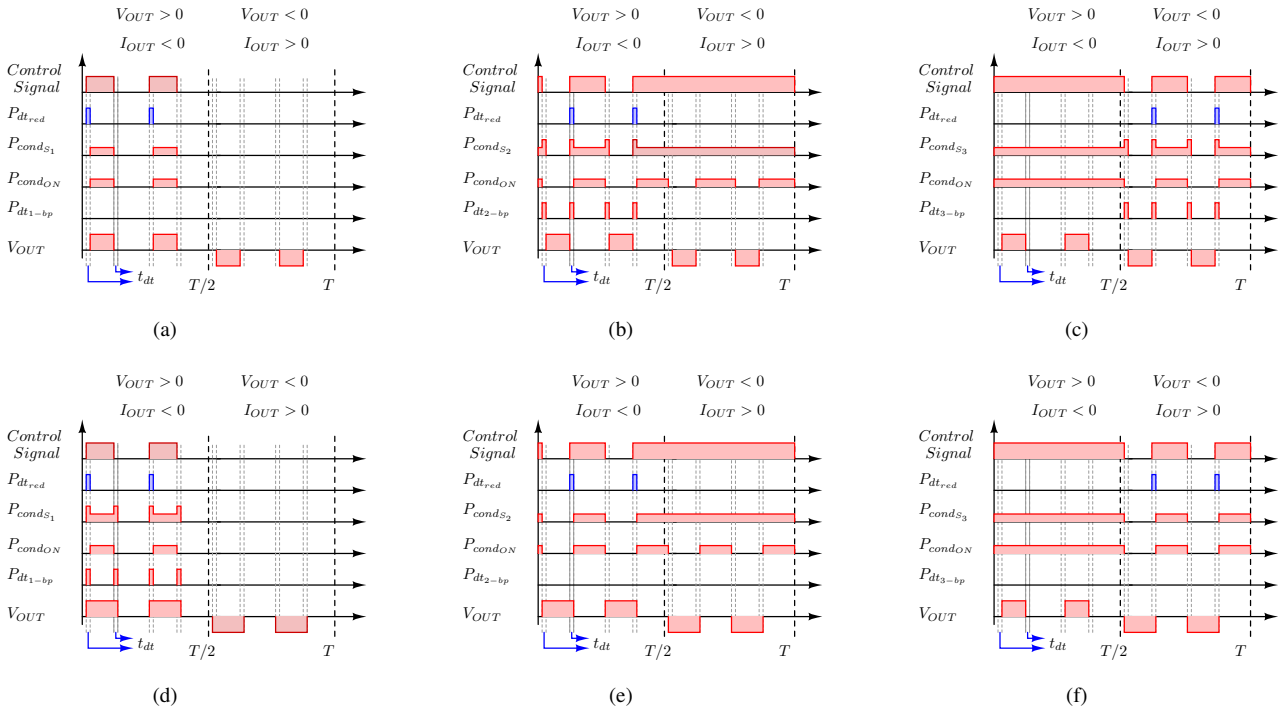


Fig. 12: Conduction instants of switches in ANPC inverter: a) S_1 switch when power factor is equal to 1, b) S_2 switch when power factor is equal to 1, c) S_3 switch when power factor is equal to 1, d) S_1 switch when power factor is equal to 0, e) S_2 switch when power factor is equal to 0, f) S_3 switch when power factor is equal to 0.

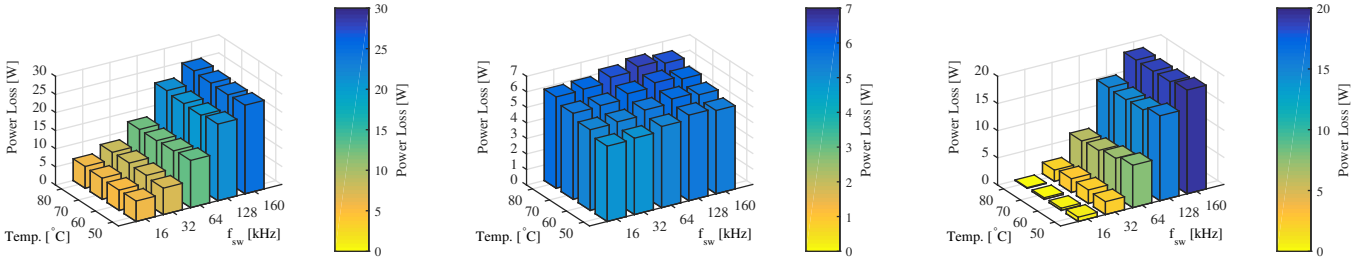


Fig. 13: Loss breakdown for GaN based ANPC converter at 1.3 kW output: a) total power cell loss, b) conduction loss, c) switching loss.

VI. Impact on Inverter Volume

The overall efficiency analysis under various output power, switching frequency and heat sink temperature conditions shows that GaN HEMTs can be used to design inverters at high frequency, high heat sink temperature conditions in order to reduce heat sink volume and output inductor volume without compromising the efficiency. In this section, the impact of high performance of GaN HEMTs on heat sink volume and output filter volume is investigated. The impact analysis is based on following assumptions:

- Cooling system is based on natural air convection.
- Single stage LC output filter is used.
- The output filter inductor current ripple is limited to 20%.
- Converter output power is rated at 2000W.

A. Heat Sink Design

The heat sink volume analysis is based on calculation of required thermal resistance r_{h_r} for heat sink at maximum output power, between 16 kHz and 160 kHz switching frequencies, and between 50 °C and 80 °C heat sink temperatures. The maximum heat sink temperature is limited to 80 °C, as the higher heat sink temperature condition may lead to exceeding maximum allowed junction temperature, which is 150 °C for GaN HEMT devices. The thermal network for ANPC inverter is illustrated in Fig. 14 where T_j is junction temperature, T_h is heat sink temperature, T_a is room temperature (chosen as 25 °C), P_{Sloss} is power loss across a single device, r_{jc} is junction-to-case thermal resistance, r_{ch} is case-to-heat sink thermal resistance and r_{h_r} is required thermal resistance of the heat sink. The junction temperature for a device T_{j_x} and required heat sink thermal resistance r_{h_r} can be calculated as

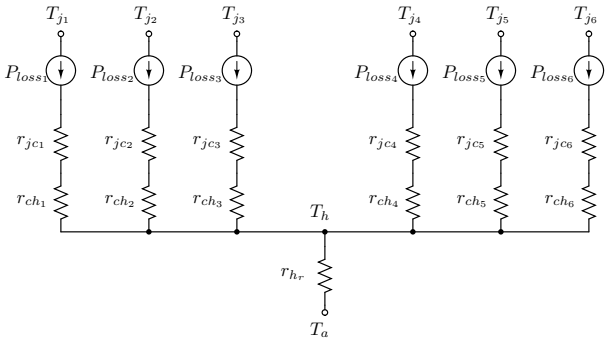


Fig. 14: Thermal network for ANPC inverter.

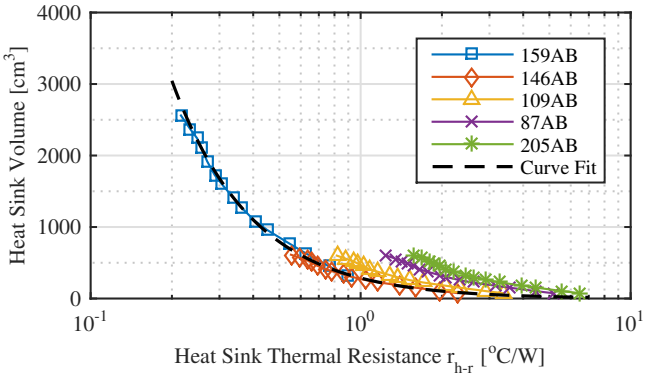


Fig. 15: Commercial naturally cooled heat sink volumes [28].

follow:

$$S_x : T_{j_x} = P_{Sloss_x} \cdot \left(r_{jc_{loss_x}} + r_{ch_{loss_x}}\right) + T_h \tag{30}$$

$$r_{h_r} = \frac{T_h - T_a}{P_t} \tag{31}$$

where P_t is total power device loss and x can be replaced with device number 1 to 6. Calculated r_{h_r} then can be used to calculate volume of heat sink based on natural air convection. The volume of various extruded naturally cooled heat sinks against heat sink thermal resistance are presented in Fig. 15 [28]. Based on the results, curve fitting is applied to minimum heat sink volume available at given r_{h_r} value and presented in Eq. 32. By using r_{h_r} from Eq. 31 in Eq. 32, volume of extruded naturally cooled heat sink can be calculated for different device case temperature, ambient temperature and power loss.

$$Vol_{heatsink} = 286.71 \cdot r_{h_r}^{-1.468} \tag{32}$$

The calculated heat sink volume with respect to switching frequency for different heat sink temperatures is presented in Fig. 16. It can be seen that the heat sink volume increases with the increase of switching frequency. The heat sink volumes at 16 kHz for 50 °C and 80 °C are 202 cm^3 and 76 cm^3 respectively. As the switching frequency is increased to 160 kHz, the heat sink volume goes up to 851 cm^3 (increase by factor of 4.21) and 290 cm^3 (increase by factor of 3.81) for these two temperature conditions. The increase in heat sink temperature from 50 °C to 80 °C provides heat sink volume

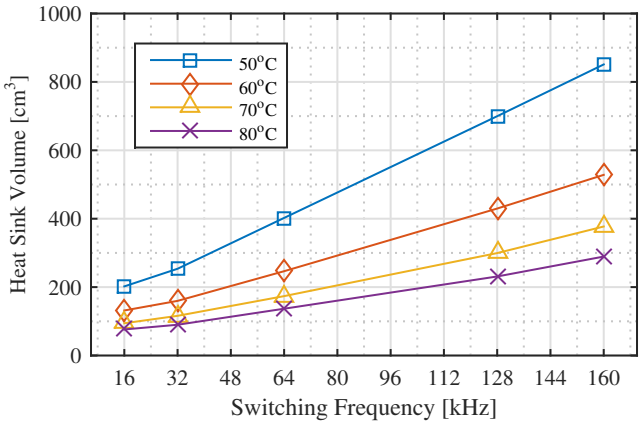


Fig. 16: Heat sink volume versus switching frequency at different heat sink temperatures.

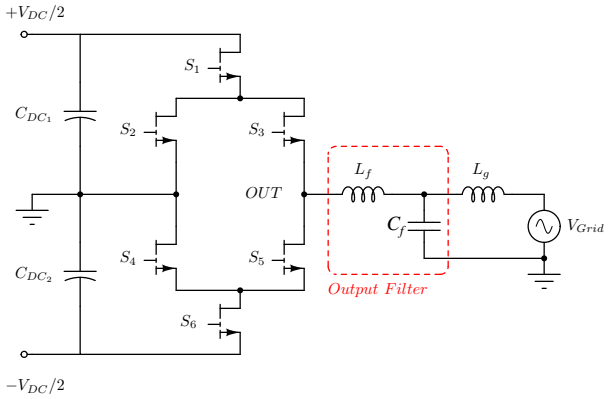


Fig. 17: Grid connected single-phase T-type inverter.

reduction by factor of 2.66 at 16 kHz, and by factor of 2.93 at 160 kHz switching frequencies. The impact of heat sink volume reduction in overall volume will be discussed after output filter design.

B. Output Filter Design

Grid connected power inverters must have an output filter in order to minimize the injected harmonics to the grid that are caused by high switching frequency. Passive filters are usually chosen in grid connected applications due to its simplicity and high performance. The size of the filter depends on number of stages and order of the filter. One of the most common type of filter is second order single stage LC filter at considered power range and presented in Fig. 17 [29]. L_{grid} in Fig. 17 is the impedance of the grid after point of common coupling and can depend on the length of grid cables, connected loads and sources to the grid.

Passive component and output filter volume is inversely proportional to switching frequency. Therefore, it is interesting to analyse the trade-off between increased power losses due to increased switching frequency and reduction in filter volume. To begin the analysis, based on Fig. 9b, the expression that defines loss of the power cell $P_{Loss_{GaN}}$ with respect to

TABLE IV: Inductance and capacitance values for output filter at different switching frequencies.

f_s	16 kHz	32 kHz	64 kHz	128 kHz	160 kHz
L_f [mH]	2.2	1.1	0.556	0.278	0.222
C_f [μF]	4.45	2.225	1.11	0.556	0.445

switching frequency f_{sw} at 2000W output power and variable heat sink temperature can be written as:

$$P_{Loss_{GaN}} = k_{t_{GaN}} \cdot (0.23015 \cdot f_{sw} + 15.6352) \tag{33}$$

where $k_{t_{GaN}}$ is:

$$k_{t_{GaN}} = 0.002855 \cdot T_h + 0.85725 \tag{34}$$

and f_{sw} is in kHz.

In this study, single stage LC filter, which is the common type differential output filter for power converters at this power range, is considered [29]. The design of LC filter starts with calculation of filter inductance L_f for defined maximum output ripple current by using Eq. 35. Calculated L_f is then used in Eq. 36 in order to calculate output capacitance:

$$L_f = \frac{V_{DC}}{8 \cdot \Delta I_{OUT} \cdot f_s} \tag{35}$$

$$C_f = \frac{1}{(2\pi \cdot f_s)^2 \cdot L_f \cdot Att_{req}} \tag{36}$$

Where V_{DC} is DC link voltage, ΔI_{OUT} is output current ripple, f_s is switching frequency and Att_{req} is required attenuation of the filter [29], [30]. The required attenuation is chosen as 0.01 in order to provide adequate damping at switching frequency and keep the resonance frequency far away from inverter switching frequency. Output ripple current is chosen as 20% of peak output current for limiting maximum power device switching current and keeping inverter output current ripple in reasonable level. Based on Eqs. 35 and 36, calculated inductance and capacitance values for different switching frequencies are presented in Table IV.

By using inductance and capacitance values in Table IV, volume of the LC filter can be calculated with area-product approach for inductor, and capacitor volume constant for capacitor. After [31], the area-product A_p and volume of a power inductor and volume can be calculated as:

$$A_p = \left[\frac{\sqrt{1+\gamma} \cdot K_i \cdot L_f \cdot \widehat{I}^2}{B_{max} \cdot K_t \cdot \sqrt{k_u \Delta T}} \right]^{\frac{8}{7}} \tag{37}$$

$$Vol_L = k_L \cdot {A_p}^{\frac{3}{4}} \tag{38}$$

where γ is ratio of iron loss to copper loss (is taken to be 0.03 or less for AC inductors with small high frequency flux ripple), B_{max} is maximum flux density in inductor core, K_i is current waveform factor ($I_{rms}/\widehat{I}$), K_t is 48.2×103, $\widehat{I}$ is peak inductor current, k_u window utilization factor (based on window fill factor, proximity and skin effects) and k_L is inductor volume constant. Maximum flux density is based on performance factor of ferrite material ($f \times B_{max}$) N87 in [32]. In this case flux density is kept at the level to achieve

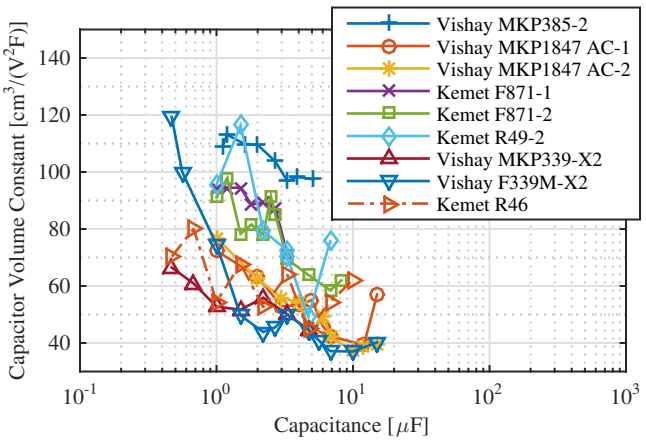


Fig. 18: Capacitor volume constant for various filter capacitors for grid connected applications.

fixed core losses at different switching frequencies. Maximum temperature rise ΔT is chosen as 60 °C in order to keep current density in the windings high enough while keeping maximum core temperature within recommended operating temperature limits. The maximum flux density for fixed core losses is approximated with the following equation:

$$B_{max} = \begin{cases} 0.35 & f_s < 25 \\ \left|1.111 \cdot 10^4 \cdot f_s^{-0.3104} - 132.3\right| \cdot 10^{-3} & 25 < f_s < 200 \end{cases} \tag{39}$$

where B_{max} is in mT and f_s is in kHz. Based on the calculated area-product value, the core with the higher closest area-product value to the calculated is selected for each switching frequency condition. After selection of the core from manufacturer data book in [32], the required air-gap in the magnetic flux path can be calculated as follow:

$$l_g = \frac{E_{stored} \cdot \mu_0}{B_{max}^2 \cdot A_e} \tag{40}$$

where A_e is effective core area, which is specified by the core manufacturer, and E_{stored} is the maximum stored energy in the core:

$$E_{stored} = 0.5 \cdot L_f \cdot \widehat{I}^2 \tag{41}$$

The reluctance of the magnetic path R is then calculated with the assumption that the permeability of the core is much higher than vacuum ($\mu_r >> \mu_0$):

$$R = \frac{l_g}{A_e \cdot \mu_0} \tag{42}$$

With the calculation of the reluctance, the required number of turns for required filter inductance can be calculated as follow:

$$N = \sqrt{L_f \cdot R} \tag{43}$$

Based on the calculated of window utilisation factor from [31], number of turns and skin effect in the windings, number of litz wires can be calculated and the appropriate wire thickness can be selected.

The next step in volume analysis of LC filter is the selection of filter capacitor. The volume of filter capacitor can be

TABLE V: Inductor, capacitor and total volume for output filter at 16, 64 and 128 kHz switching frequencies.

f_s	16 kHz	64 kHz	128 kHz
Inductor Volume [cm^3]	266.3	141.7	96.4
Capacitor Volume [cm^3]	20.2	5.1	4
Total Volume [cm^3]	286.5	146.8	100.4

calculated by the following equation:

$$Vol_C = k_c \cdot C_f \cdot {V_{nom}}^2 \tag{44}$$

Where V_{nom} is nominal voltage of capacitor and k_c is capacitor volume constant in $cm^3/\left(V^2F\right)$. A survey is conducted to evaluate the volume of capacitors for grid connected output filter applications (X2 type) and the capacitor volume constant of different capacitors from different manufacturers are presented in Fig. 18. It can be seen that the k_c varies for different manufacturers and also capacitance values. The MKP339-X2 series is selected as it has the lowest k_c over wide range of capacitance [33]. The k_c for MKP339-X2 series is approximated as 60.

The inductor and capacitor volumes for each switching frequency case in Table IV are calculated using Eqs. 35 - 44. Based on the calculation results, three filter cases have been realised for 16 kHz, 64 kHz and 128 kHz switching frequencies. The realised filters are presented in Fig. 19 and the inductor volume, capacitor volume and total filter volume values are presented in Table V. It should be noted that the calculated exact capacitance value according to Eq. 36 cannot be purchased, therefore the closest values to the ones presented in Table IV (4.7 μF for 16 kHz, 1 μF for 64 kHz and 680 nF for 128 kHz) are used.

The comparison of the calculated and realised volumes for the inductor, capacitor and total filter are presented in Fig. 20a. It can be seen that the calculated values for inductor and capacitor are well matched with the realised filter. In Fig. 20a, it is also shown that the total filter volume is dominated by the inductor volume and the rate of volume reduction for the inductor reduces beyond 64 kHz. The total filter volume can be reduced by factor of 2 with the increase of switching frequency from 16 kHz to 64 kHz. The factor of reduction increases to 2.86 as the switching frequency is increased to 128 kHz. There are two reasons for reduction in rate of reduction beyond 64 kHz: 1) The increase of core size as the core losses is aimed to be kept constant, 2) The reduction of fill factor in winding area due to increase of skin effect. The skin effect causes increase in number of wires in parallel and reduction in wire diameter to achieve low AC resistance at given switching frequency with desired current density in the winding.

The performance of the designed filter inductors are evaluated at 1.6 kW output power at their designed switching frequencies: 16 kHz, 64 kHz and 128 kHz. The output power is kept constant for each test condition by slight increase in modulation index due to fixed dead-time and the heat sink temperature is kept at 30 °C. The loss results in Fig. 20b shows that the efficiency of the power cell or the filter is not compromised with reduction of output filter size. The filter

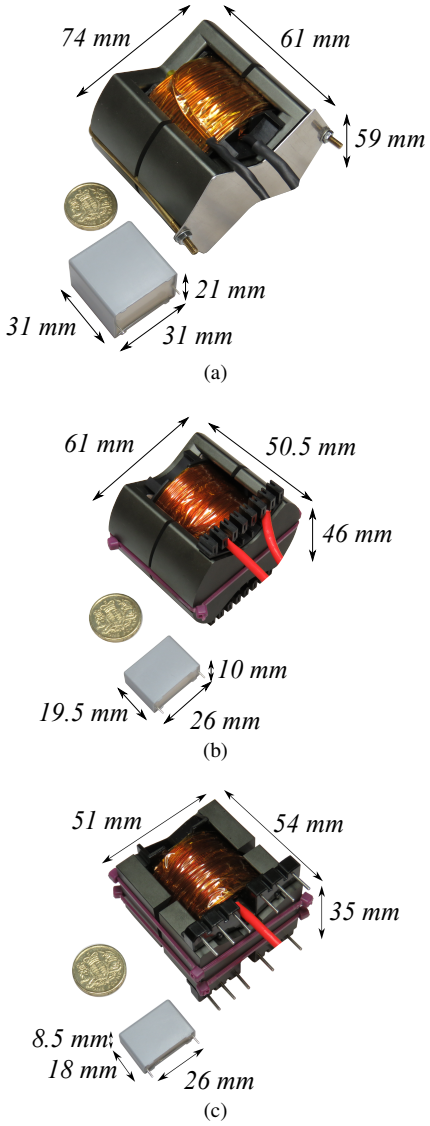
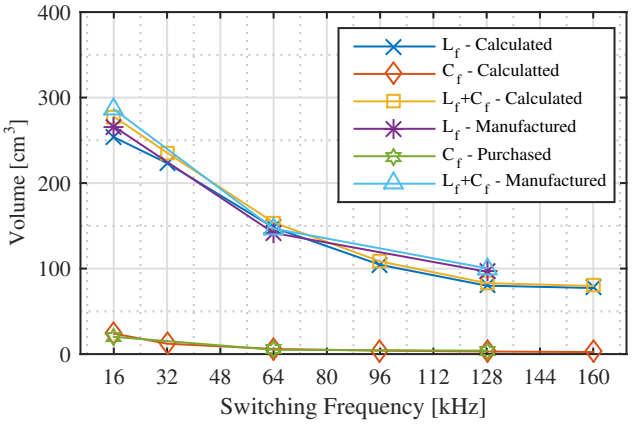


Fig. 19: Designed LC filters for three different switching frequencies: a) 16 kHz b) 64 kHz and c) 128 kHz.

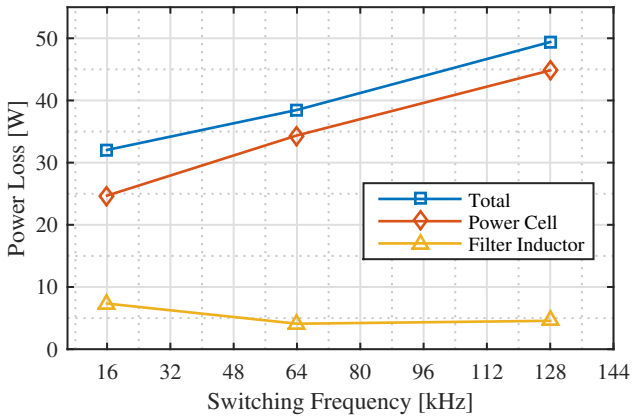
inductor loss is almost constant at 64 kHz and 128 kHz, and smaller than at 16 kHz due to reduced number of turns.

In order to include the temperature and power cell loss impact to the volume reduction analysis, the filter volume, heat sink volume and the total volume of filter and heat sink volume are presented with respect to switching frequency at different heat sink temperatures in Figs. 21a and 21b. It can be seen that heat sink volume is almost equal to filter volume at 32 kHz, 50 °C and dominates the total volume beyond 32 kHz in Fig. 22a. When the heat sink temperature is increased to 80 °C, as shown in Fig. 21b, the filter and heat sink volume crosses around 64 kHz. The overall comparison in Fig. 22a shows that the increased heat sink temperature can bring significant volume reduction at switching frequencies above 64 kHz and low heat sink temperatures such as 50 °C and 60 °C can lead to increase in overall volume as the heat sink dominates the total volume.

Finally total volume is plotted with respect to switching

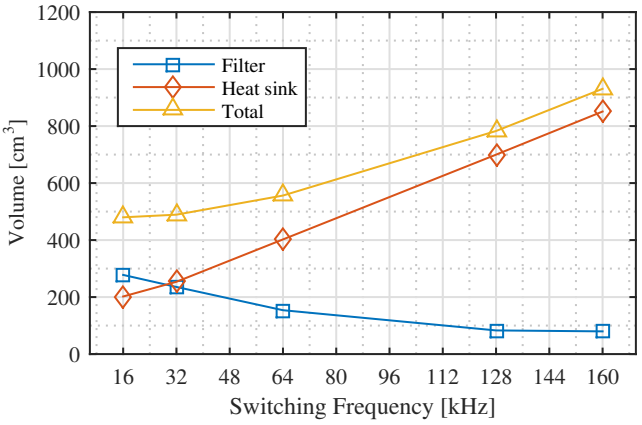


(a)

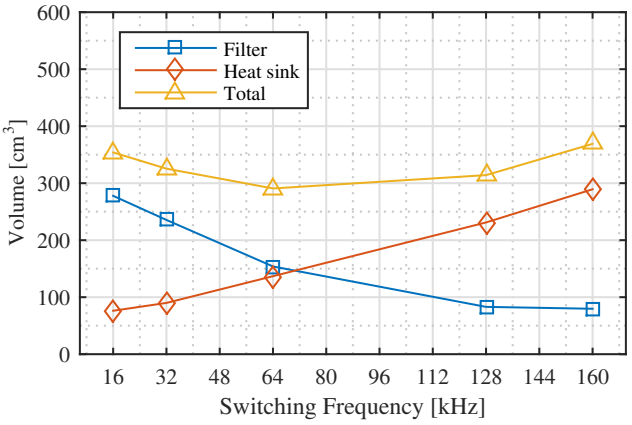


(b)

Fig. 20: a) Calculated and realised inductor, capacitor and total filter volume versus switching frequency, b) Total, power cell and inductor loss at 64 kHz and 128 kHz switching frequencies.



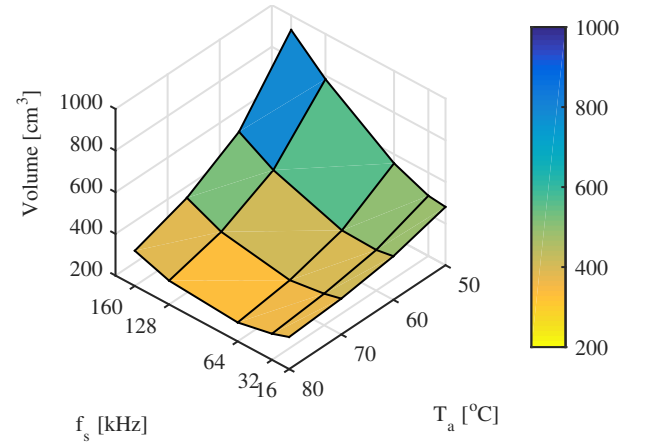
(a)



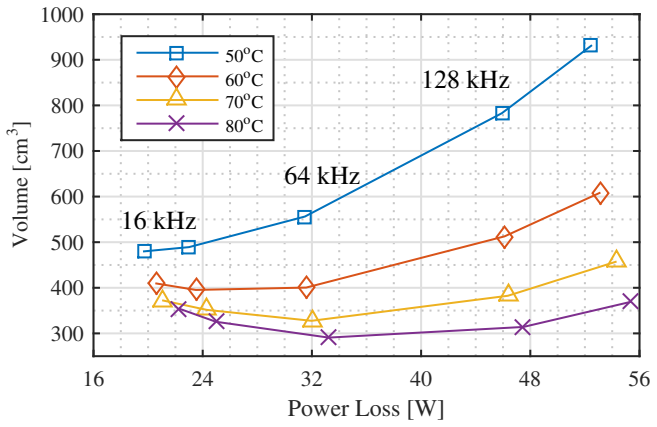
(b)

Fig. 21: Filter, heat sink and total volume versus switching frequency: a) at 50 °C heat sink temperature and b) at 80 °CC heat sink temperature.

frequency and heat sink temperature in Fig. 22a, and with respect to power cell loss at different heat sink temperatures in Fig. 22b to give an overall summary of impact of GaN HEMT performance in heat sink and output filter volume. It can be seen in Fig. 22a that the increase of switching frequency lead to increase of total volume at low heat sink temperatures due to increase in heat sink size, and at high heat sink temperatures, increase of switching frequency beyond 64 kHz does not lead to significant decrease in total volume. Contrary, above 128 kHz the total volume starts to increase again due to heat sink volume increase. In terms of the comparison of total volume and power loss, Fig. 22b shows that at 50 °C, increase of power loss by factor of 1.6 times (16 kHz to 64 kHz) leads to increase in total volume by 1.16 times. On the other hand, at 80 °C, increase of power loss by factor of 1.5 times (16 kHz to 64 kHz) leads to decrease in total volume by 1.22 times.



(a)



(b)

Fig. 22: a) Total volume versus switching frequency and heat sink temperature, b) total volume versus power cell loss.

VII. Conclusion

In this paper, the impact of GaN HEMT to a single phase inverter in terms of power loss, converter efficiency, heat sink and output filter volume is discussed. It is shown that the GaN HEMT has excellent switching and conduction performance under different load and heat sink temperature conditions that results in very high efficiency and low power cell loss. Therefore, the the findings from static, dynamic characterisation and single phase prototype results clearly show that GaN HEMT has excellent switching performance under wide load current and heat sink temperature conditions. The high performance of the inverter, thanks to GaN HEMTs, lead to reduction of total volume, including output filter and heat sink volume, by factor of 1.22 times with increase of switching frequency from 16 kHz to 64 kHz, and increase of heat sink temperature from 50 °C to 80 °C.

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